Phase-Dependent Single-Event Sensitivity Analysis of High-Speed A/MS Circuits Extracted from Asynchronous Measurements

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***Abstract*—A method for experimental determination of the phase dependence of single-event sensitivity in high-speed A/MS circuits is presented. The technique ensures testing coverage of the complete data cycle and results in a correlation of errors to the data or clock cycle of the circuit. Designers can apply the information, along with knowledge of the circuit state at the time of errors, to make informed radiation-hardening-by-design decisions.**

***Index Terms*—High speed integrated circuit measurements, semiconductor device radiation effects, single event effects.**

I. Introduction

THE testing of highly-scaled state-of-the-art integrated circuits (ICs) for single event effects (SEEs) is one of the more challenging problems facing the radiation-effects community today. We have been developing time-domain, laser-based SEE test approaches for high-speed SerDes and phase lock loop (PLL) devices that are applicable to other high-speed circuits: analog, mixed-signal, and digital. Advantages of the time-domain approach include the ability to characterize the full range of single-event error signatures, even varying program-to-program requirements, and to gather a data set that allows significant flexibility in terms of post-processing of the data beyond error identification and characterization.

It is well understood that single-event transients (SETs) in combinational logic are captured (latched) only when the SET arrives during some fraction of a clock cycle (near the clock edge). This sensitive time period is referred to as the window of vulnerability (WOV), and varies with the clock frequency and the charge generated by the ionizing event [1]. Determining the window of vulnerability in an experimental setting is difficult, especially for circuits operating at high frequencies. The WOV parameter is rarely measured experimentally due to the complexity of synchronizing the circuit clock with a repetitive ionizing event. This measurement is especially difficult in broad-beam accelerator experiments.

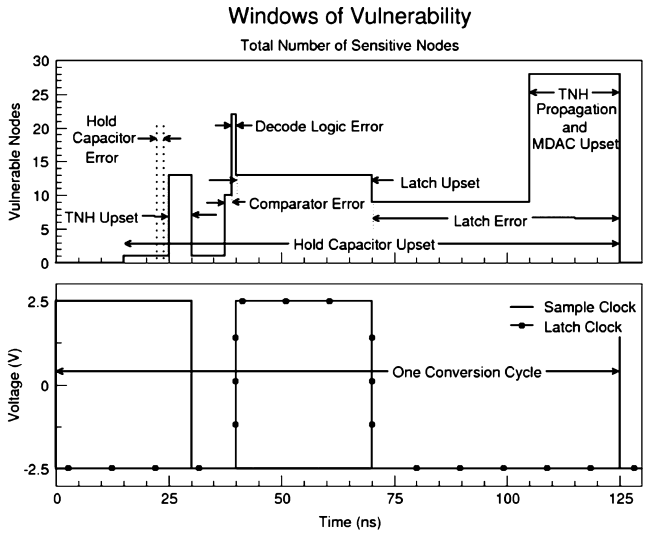

Fig. 1. Example of a simulated system WOV. The bottom figure shows the conversion cycle for a system. The top figure shows the source of errors or upsets, the number of nodes that elicit that response, and the duration with respect to the conversion cycle for which the error is likely. The proposed technique will enable an easy method to experimentally extract similar information from high-speed devices. Figure from [2][1].

When referring to analog circuitry, WOV is a misnomer because the sensitivity of the circuit is measured with respect to the phase of the data cycle as opposed to time in relation to the clock. In this paper, the vulnerability of the device is described as the phase-dependent sensitivity (PDS). The WOV nomenclature is used only when referring to digital circuitry or referencing previous works that use the acronym. PDS is used throughout to reference sensitivities in analog, mixed-signal, as well as digital circuits.

In this paper we take advantage of the intrinsic asynchronous nature of laser-induced SEE experimental approaches and demonstrate a new method for experimentally extracting the phase sensitivity of a circuit. The results presented here illustrate the utilization of the time-domain via a laser data collection technique in which multiple transients are collected

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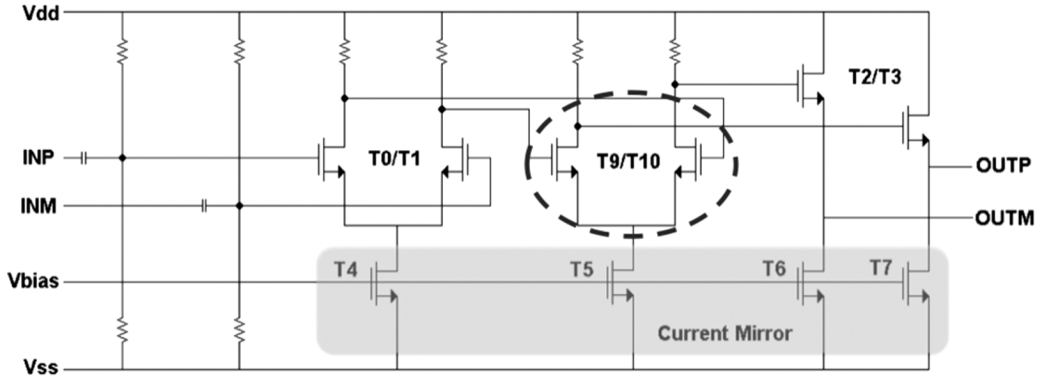

Fig. 2. Pre-emphasis schematic for illustration of the application of the data gleaned from the phase-dependence information. When OUTP is high (the vulnerable portion of the circuit), T9 is off.

at each location in a laser scan. The intrinsic asynchronous characteristic of the experimental setup allows an examination of phase-dependent circuit behavior to extract the PDS, eliminating the complexities associated with synchronizing the circuit to the experiment. Detailed characterization of the parameter space that affects the PDS in high-speed circuits is made possible and the analysis provides a tool to improve future RHBD circuit designs.

II. Background

The challenges faced in the SEE testing of highly scaled, high-speed circuitry are formidable. Error rates are often determined using a bit error rate tester (BERT), but if the temporal characteristics of the errors are of interest, a time-domain error-identification method must be used. An oscilloscope triggered on an error event is often used to capture the transients using pre-defined criteria based on error traits predicted for a specific system. In heavy-ion environments, this error-triggering method is practical but can lead to overlooked errors if the error signature is different than expected, e.g., the occurrence of a phase error when triggering off the temporal characteristics of a missed bit. In the case of a repetitive ionizing event such as that of a laser test, it is possible to trigger the oscilloscope on the laser pulse to collect a data set without presumption of error characteristics.

Previous work describes a technique for determining the WOV in combinational logic via a pulsed laser synchronized with the circuit clock [1] and determining the WOV through a simulation technique [2]. The experimental technique is not widely used because of the complexities in matching the circuit clock to the laser operating frequency, particularly in today's high-speed circuits. As a case in point, in most picosecond and femtosecond laser systems, the laser pulse repetition rate is synchronized to a master oscillator and, therefore, is not tunable. In such cases, synchronization with the operating frequency of the circuit is difficult or impossible.

SEE simulations are extensively used and can be valuable in determining the WOV. However, they cannot provide the confidence achieved through experimental characterization. An example of a simulated WOV diagram for a system is shown in Fig. 1. The top frame denotes the source of upsets and errors in a combinational logic circuit, the number of sensitive nodes for each error type, and the time period within a conversion cycle (shown in the bottom frame) in which the vulnerable nodes are sensitive to SEEs. This figure illustrates the complex nature of the WOV in modern circuits and implies the difficulty in experimentally extracting such detailed information, thus motivating this work. This paper illustrates a method of postprocessing large amounts of experimental data collected in a manageable, asynchronous manner devoid of complex timing constraints in order to extract the equivalent of this figure for complex analog circuit SET characterization.

III. Analysis Technique

A. Data Collection

This work utilizes data collected via a technique described in [3] in which periodic laser pulses are used as an oscilloscope trigger to record data from a circuit operating at a frequency independent of the repetition rate of the laser. The through-wafer TPA single-event upset (SEU) mapping technique, as described in [4]–[6], is used to perform SET characterization of the circuit. The TPA SEE experimental setup is described in [7] and [8].

The majority of the data for this paper is from experiments on a pre-emphasis amplifier from a serializer-deserializer (SerDes) device designed in IBM's 90 nm CMOS9SF process (Fig. 2). The circuit is operated at 3.16 Gbps with a 400 mV peak-to-peak differential sinusoidal input voltage, which, for this proof-of-concept paper can be interpreted as either a checkerboard data pattern or a clock signal.

Errors are injected by scanning the laser across the T9/T10 differential amplifier (Fig. 2) in 0.3 μm steps at an incident laser pulse energy of 4.63 nJ—sufficiently above threshold to produce SETs without saturating the error response. An automated data collection setup controls the x-y position of the device and captures data from the oscilloscope with little interaction from the operator. For each step in the scan, multiple transients triggered off the repeating laser strikes are recorded using a Tektronix 12 GHz TDS6124 oscilloscope operating with a resolution of 20 GS/s. For each transient event, data points are recorded with adequate oscilloscope resolution at the time of the laser strike to allow accurate analysis.

[1]The acronym 'TNH' in the top panel of the figure stands for track-and-hold, referencing a subcircuit in the simulated system.

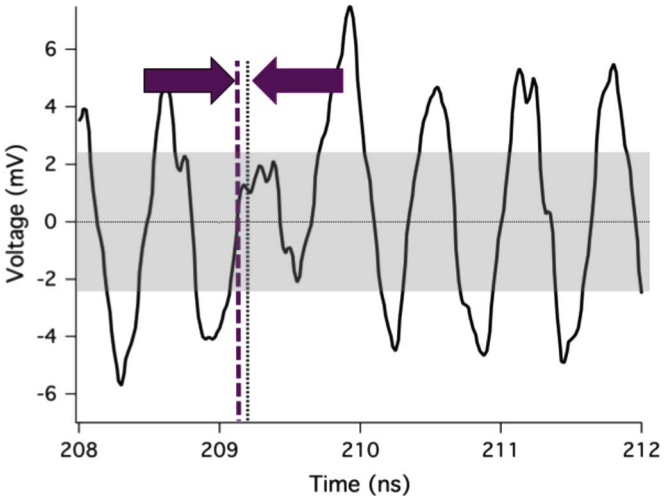

Fig. 3. Schematic diagram illustrating the process for determining the strike time in the clock cycle. The time difference between the zero crossing (left vertical line) and the laser strike time (right vertical line) defines the phase relationship of each trace relative to the error injection and is determined by a computer scripted process.

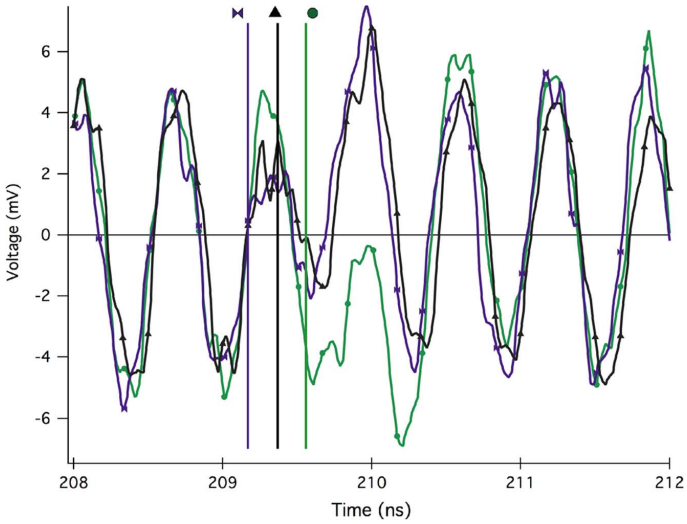

Fig. 4. Three traces lined up in phase to directly illustrate the difference in response with laser strikes at different times in the data cycle. The vertical lines indicate the time of the laser strike for each individual trace. The times between the aligned zero crossing and the respective strike are collected for further analysis.

In this experimental approach the oscilloscope and laser are allowed to run with each operating at its own characteristic frequency. Consequently, the phase relationship between the two signals will vary with time, resulting in error injection at varying, random points within the data cycle. If enough events are recorded at a given location in the circuit, the injected errors will span the entire data cycle, ensuring sampling of the "worst-case" scenario with respect to the phase of the data is captured.

B. Data Analysis

A data analysis program has been written to determine the elapsed time between the rising edge of the data and the laser strike of each signal stream (Fig. 3). Another way to visualize the outcome of this process in seen in Fig. 4 in which the rising edge of the data cycles have been aligned and the times of the corresponding laser strikes are identified by vertical lines. The extracted Δt values are converted to a phase value (between 0 and 2π) and binned in a histogram to ensure sufficient data are collected to have a uniform distribution of laser strikes across the data cycle. This metric is demonstrated with the histogram of the pre-emphasis circuit data (Fig. 5).

During data analysis, errors are processed based on the characteristics observed during the testing process using thresholds determined by the constraints of the application. In the example situation, the script checks for bits that do not meet a user-defined voltage threshold criterion (see shaded region of Fig. 3). In the case of a PLL circuit, errors are identified as shifts in the frequency of the clock [9]. When errors are identified, the corresponding Δt values are binned as described for Fig. 5. The resulting histogram identifies the phase(s) of the data cycle for which the laser irradiation produced errors, thus providing the PDS. Fig. 6 illustrates the PDS plot, described further below.

In addition to the described experiment, data were obtained using the same technique for two other circuit scenarios: the pre-emphasis circuit operating at 2 Gbps with a 4.63 nJ incident laser pulse energy, and a charge pump circuit of a PLL operating at 150 MHz scanned with a 3.5 nJ incident laser pulse energy.

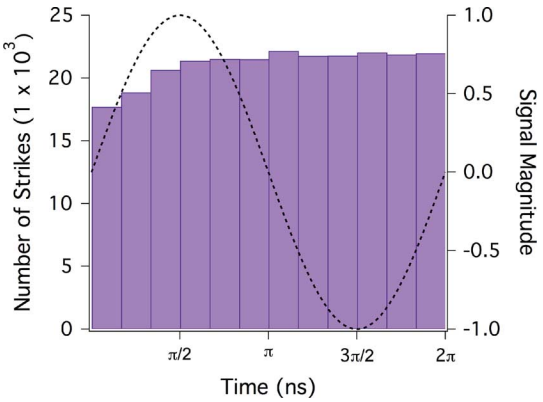

Fig. 5. Distribution of strike times over the data cycle. Taken from a test of the circuit in Fig. 2.

IV. Application

The determination of the single-event PDS provides to the designer information that may be used to analyze vulnerabilities of circuits and improve future designs. The knowledge of the phase sensitivity and the resulting outputs provides insight to the specific operating condition of the circuit at the time of errors. PDS results from a pre-emphasis amplifier in a SerDes device and a NMOS switch in a charge pump of a PLL are described in this section.

A. Pre-Emphasis Amplifier in a SerDes Device

The circuit shown in Fig. 2 is used as the preliminary example of the technique because of the straightforward design. All of the presented data is from laser irradiation of the T9/T10 differential amplifier, which has been identified as the most sensitive region of the circuit [3]. Errors are defined as local maxima or minima

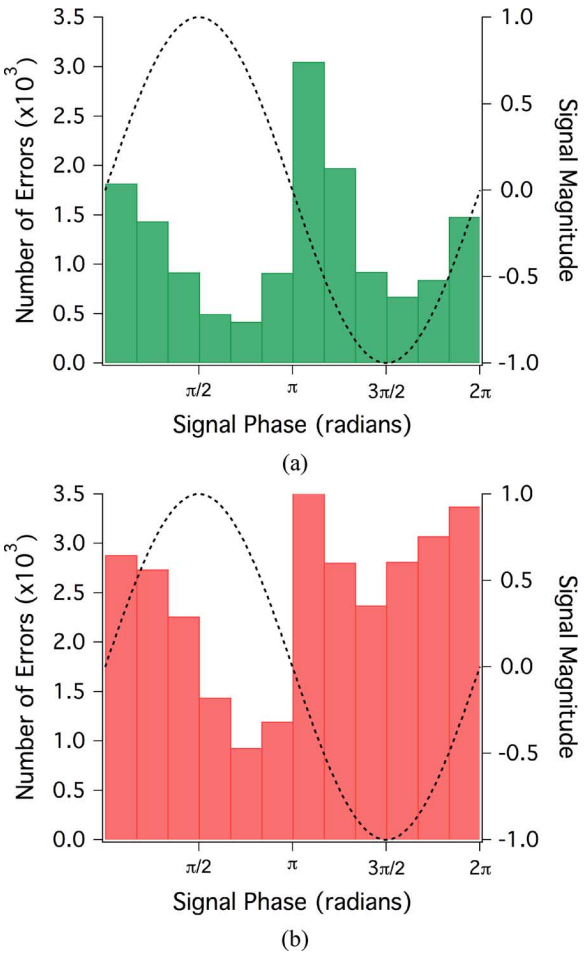

Fig. 6. Histograms of error counts superimposed on the data cycle for the outputs of a scan of the device operating at 2 Gbps with an incident laser energy of 4.63 nJ. OUTP (a) shows fewer errors overall than (b) OUTM due to excess noise on the OUTM signal. Errors are binned according to the time in the data cycle the laser struck the device.

with values less than 50% of the average maximum or minimum voltage of the transient.

Fig. 6 shows the number of errors in the scan binned with respect to the time of the laser strike in the data cycle. A sinusoidal signal with ideal output characteristics is overlaid for correlation with the binned data. The vulnerable portion of the data cycle is shown for the positive (Fig. 6(a)) and negative (Fig. 6(b)) outputs of the circuit (OUTP and OUTM, respectively) during a scan of the differential-pair transistors T9 and T10. The error profiles for the two outputs indicate the sensitive time in the cycle as the negative portion of the cycle, i.e., data LOW.

The PDS data provides the designer with a tool to determine the vulnerable percentage of the data cycle and assess the operating state of the scanned device during the vulnerable time, similar to the knowledge gained when performing a WOV analysis of a digital circuit. As an example, the data presented in Fig. 6 show errors concentrated in the latter portion of the data cycle. Through circuit analysis (see Fig. 2) and from knowledge of the test setup, the cause for the errors is related to the biasing of the circuit. During the experiment, T9 and T10 were biased in such a way that when one side of the differential amplifier is pulling the majority of the tail current (during the extremes of the data cycle), the other transistor falls into the ohmic operating region. Any perturbation due to single events on the gate of a transistor operating in the ohmic region causes large fluctuations in current in the ohmic device. The disparity in number of errors between the OUTP and OUTM data is due to the area of T9 being truncated during the scan.

Using this information, an informed decision as to the proper hardening technique can be made. In this case, a change in the biasing of the differential amplifier would be prescribed to allow the circuit to operate in saturation throughout the data cycle.

B. NMOS Output Switch in PLL

Data from a 3.5 nJ TPA scan of a PLL circuit (designed using the IBM 130 nm CMRF8SF process) are analyzed for single-event-induced jitter response and identified errors are binned with respect to the strike time in the 150 MHz data cycle. Previous works have indicated the extreme single-event vulnerability of the charge pump sub-circuit with respect to the other PLL components; data were therefore collected for strikes in the charge pump as they impact the PLL output [5], [10].

A layout view of the charge pump sub-circuit and corresponding schematic are shown in Fig. 7(a) and (b), respectively [10]. Moreover, a 2-dimensional (2-D) mapping showing the magnitudes of the output phase jitter (displacement) resulting from strikes in various portions of the circuit are overlaid on the layout view. The 2D-mapping was performed as a function of x-y location using a step size of 0.2 μm. Each x-y point represents the average phase displacement of ten transient perturbations.

The most vulnerable transistors in the charge pump (those resulting in the largest jitter values) were the NMOS transistors in the two output switches. This vulnerability arises from the direct connection of the output switch to the control voltage, V_{inVCO}, of the voltage-controlled oscillator (VCO) circuit. Thus, any charge deposited onto the output node directly modifies the control voltage and the resulting output frequency of the PLL. Strikes on the PMOS devices also result in significant phase error, however at less severity due to the high frequency limitations in the bandwidth of the PLL. Strikes on the PMOS devices increase the instantaneous output frequency, whereas strikes on the NMOS devices lower the instantaneous output frequency (output frequency can be reduced to approximately 0 Hz) [10]. The pull-up (PMOS) and pull-down (NMOS) current sources also result in observable phase jitter, though with less impact as the output switches filter the response.

The PDS for strikes on the NMOS switches in the charge pump is plotted in Fig. 8 as the number of errors with respect to cycle time. Upsets are observable across the entire clock cycle because the output switches are directly connected to the VCO control voltage. However, errors tend to be concentrated about the rising and falling edges of the clock cycle, as observed by the sharp peaks in the distribution. The phase jitter and SE displacement are calculated at the cycle edges, therefore, strikes timed to the clock edges result in a more immediate shift in the output frequency of the VCO. Strikes timed to the center of the clock cycle will also result in an apparent stretching or compressing

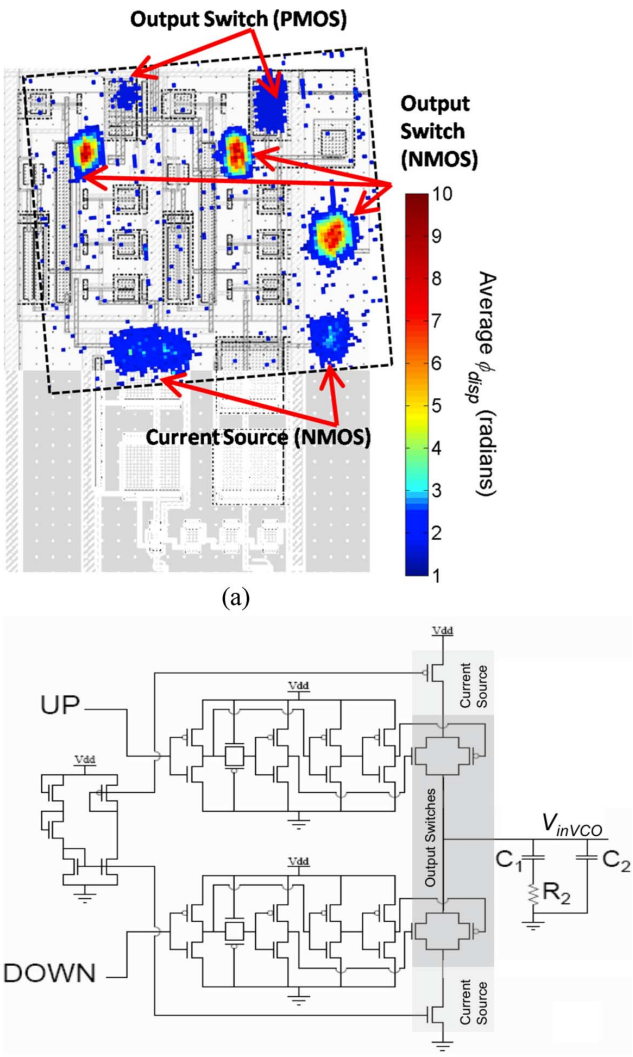

Fig. 7. (a) TPA scan showing phase-displacement results for the PLL. The right-most NMOS output switch is the source of the presented data. Figure from [10]. (b) Schematic of charge pump indicating output switches and current sources.

of the output signal, however will be slightly damped due to the delayed effect until the next observable clock edge.

V. Conclusion

A method for experimental determination of the phase dependent sensitivity (PDS) of high-speed circuits is presented. The proposed analysis permits the determination of the sensitive times in the data cycle through collection of multiple transients when the circuit is operating asynchronously with the trigger signal. The lack of a phase relationship between the laser and the circuit results in error injection at random points in the cycle, permitting a complete mapping of the error susceptibility throughout the data (clock) cycle of the circuit. This is the phase-dependent sensitivity (PDS) of the circuit. This technique provides enhanced understanding of the SET response of the device.

The visualizations of the data allow the designer to more fully understand the behavior of the circuit by providing a point of reference for the likelihood that an error will occur relative to the timing of the circuit. This, along with knowledge of the circuit state at the time of errors, helps identify the mechanism causing the error and leads to targeted design improvements. In addition, the analysis technique can be used to determine the vulnerable percentage of the data cycle, which can be used to aid in the estimation of the error rate. With careful planning, this flexible data set and analysis technique can reduce the amount of time required for circuit iteration. The ease in the experimental determination of the phase-dependence of the circuit demonstrated here illustrates the intrinsic advantages of the time-domain laser SEE approaches developed previously [3], and should enable this metric to be more widely utilized in the future.

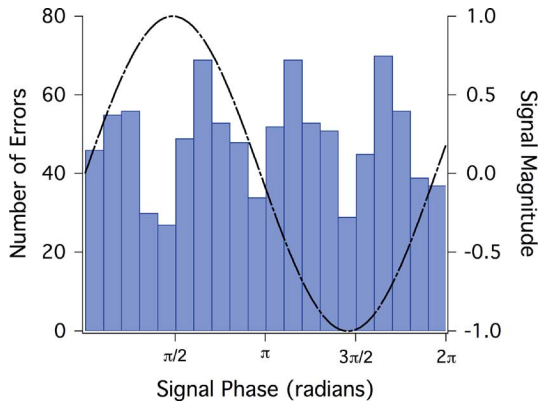

Fig. 8. Number of errors with respect to cycle time for NMOS switches in a PLL. Note that the number of errors correlates to the rising and falling edges in the overlaid data cycle.

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